



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|--|-------------|----------------------|---------------------|------------------|
| 10/081,818 | 02/20/2002 | Jerome M. Eldridge | 1303.045US1 | 3148 |
| 21186 | 7590 | 03/24/2006 | EXAMINER | |
| SCHWEGMAN, LUNDBERG, WOESSNER & KLUTH 1600 TCF TOWER 121 SOUTH EIGHT STREET MINNEAPOLIS, MN 55402 | | | HO, TU TU V | |
| | | | ART UNIT | PAPER NUMBER |
| | | | 2818 | |

DATE MAILED: 03/24/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

HA

| | | | |
|------------------------------|------------------------|---------------------|--|
| Office Action Summary | Application No. | Applicant(s) | |
| | 10/081,818 | ELDRIDGE ET AL. | |
| | Examiner | Art Unit | |
| | Tu-Tu Ho | 2818 | |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 10 March 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-23 and 85-96 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☒ Claim(s) 16,17,19 and 87-95 is/are allowed.
- 6) ☒ Claim(s) 1-15,18,20-23,85,86 and 96 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 20 February 2002 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
 2. ☐ Certified copies of the priority documents have been received in Application No. _____.
 3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input checked="" type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 03/06/2006 has been entered.

Claim Rejections - 35 USC § 103

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

2. **Claim 1, 3, 4, 7-9, 18, and 96** are rejected under 35 U.S.C. §103(a) as being unpatentable over Endo U.S. Patent 5,619,051 (the '051 reference, cited in a previous office action) in view of Werkhoven et al. U.S. Patent Application Publication 20010041250.

The '051 reference discloses a floating gate transistor as claimed including a graded asymmetrical low tunnel barrier intergate insulator 18A but does not teach that the graded asymmetrical low tunnel barrier intergate insulator 18A is formed by multiple atomic layer deposition (ALD). Instead, the reference teaches that the graded asymmetrical low tunnel barrier intergate insulator 18A is formed by chemical vapor deposition (CVD).

Specifically, with reference to **claims 1 and 18**, the '051 reference discloses a floating gate transistor, comprising:

a first source/drain region (22 or 24, Fig. 5) and a second source/drain region (24 or 22) separated by a channel region (no number) in a substrate (10);

a floating gate (16) opposing the channel region and separated therefrom by a gate oxide (14);

a control gate (20) opposing the floating gate; and

wherein the control gate is separated from the floating gate by an asymmetrical low tunnel barrier intergate insulator (18A, wherein “the dielectric film 18A is formed of a solid solution of two kinds of metal oxides, and the proportions of two metal oxides vary continuously from the bottom plane adjacent to the floating gate 16 to the top plane”, column 7, lines 1-8, so as to produce different barrier heights (represented by different band widths, col. 7, lines 55-67), meeting the limitation “graded” and “asymmetrical”, where “low” is interpreted broadly, and where the “tunnel barrier” property is interpreted to be inherent as the stepwise-graded dielectric layer 18A is a barrier to, for example, electrons tunneling from, for example, from the floating gate to, for example, the control gate).

However, as noted above, the reference discloses that the graded asymmetrical low tunnel barrier intergate insulator 18A is formed by CVD instead of multiple ALD as claimed.

Werkhoven, in also disclosing an insulator (“dielectric”), and particularly an insulator for a transistor gate (gate oxide/Si substrate interface or gate electrode/gate dielectric interface, paragraph [0034]), teaches that an insulator formed by multiple ALD is superior to CVD in that its thickness, grading, and compositional ratios can be exactly controlled, in addition to the reduced problem of diffusion (paragraphs [0033]-[0036]).

Art Unit: 2818

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the reference's device such that its graded asymmetrical low tunnel barrier intergate insulator 18A is formed by multiple ALD instead of CVD.

One would have been motivated to make such a change in view of the teachings in Werkhoven that multiple ALD is superior to CVD in terms of precisely controlled thickness, grading, compositional ratios, and reduced diffusion.

Referring to **claims 7-8 and 18**, the '051 reference in view of Werkhoven discloses a non volatile memory cell substantially as claimed and as detailed above for claim 1 including the asymmetrical low tunnel barrier intergate insulator 18A including a number of small compositional ranges arranged in a "vary continuously" from the bottom surface to the top surface. The reference further discloses, in reference to **claim 18**, that the number of small compositional ranges is formed such that gradients can be formed in an applied electric field which produce different barrier heights at an interface with the floating gate and control gate (paragraph bridging columns 7 and 8, particularly "...gradient of conduction band to make an about 0.4 eV difference...information charge retention time is about twice that in the memory cell of FIG. 1...the erase time shortens to 1/5 of that in the memory cell having the dielectric film 18 of homogeneous barium strontium titanate).

The reference further teaches that the floating gate includes a polysilicon floating gate having a metal silicide formed thereon (column 3, lines 56-63) in contact with the asymmetrical low tunnel barrier intergate insulator, and that the control gate includes a metal control gate having a metal oxide layer formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator.

Compared with the claims, the reference discloses a metal silicide instead of the claimed first metal layer for the floating gate, a metal oxide/metal instead of the claimed second metal/polysilicon for the control gate. However, the differences are deemed to be obvious to one of ordinary skill in the art at the time the invention was made (“the artisan”) because at least one of the following two reasons: (1) the materials are known and available to the artisan; (2) both the present invention and the reference fails to show an advantage of one combination of materials to the other.

With respect to the limitation “wherein the metal layer includes a metal layer that has a different work function than the metal layer formed on the floating gate”, the limitation appears to be inherent in the reference because: (1) the metal of the metal silicide (functionally equivalent to the claimed first metal) and the metal of the metal oxide (functionally equivalent to the claimed second metal) are different metals, resulting in different work functions; (2) the paragraph bridging columns 7 and 8, as noted above, expressly states that the barrier heights at the two surfaces of the asymmetrical low tunnel barrier intergate insulator, where the metal silicide and the metal oxide are respectively in contact with, ought to be different, leading the artisan to conclude that the work function of the metal silicide (functionally equivalent to the claimed first metal) should be different from the work function of the metal oxide (functionally equivalent to the claimed second metal).

Referring to **claim 3**, the reference further discloses that the graded asymmetrical low tunnel barrier intergate insulator includes an asymmetrical transition metal oxide, as SrTiO_3 (column 7, lines 9-12) is a transition metal oxide.

Art Unit: 2818

Referring to **claim 4**, although the reference's transition metal oxide is formed of a transition metal not the same as one of the claimed transition metals, they are all transition metals, therefore their metal oxides should be functionally equivalent.

Referring to **claim 9**, although the reference does not explicitly disclose that the floating gate transistor is an n-channel type floating gate transistor, one of ordinary skill in the art recognizes that an n-channel type floating gate transistor and a p-channel type floating gate transistor are only different in the dopants (n or p) used.

Referring to **claim 96**, the graded asymmetrical low tunnel barrier intergate insulator formed by multiple ALD should be continuously graded, as ALD is about atomic level deposition, i.e., one atomic layer (otherwise known as a monolayer) deposited at a time upon a previously deposited monolayer and because both the '051 reference and Werkhoven teach continuously grading.

3. **Claims 10, 11, 14-15, and 23** are rejected under 35 U.S.C. 103(a) as being unpatentable over Endo U.S. Patent 5,619,051 (the '051 reference, cited in a previous office action) in view of Werkhoven et al. U.S. Patent Application Publication 20010041250 and further in view of Orłowski et al. U.S. Patent 6,433,382 (cited in a previous office action).

Referring to **claims 10 and 23**, the '051 reference discloses a non volatile memory cell substantially as claimed including the graded asymmetrical low tunnel barrier intergate insulator 18A formed by multiple ALD in view of Werkhoven as detailed above for claims 1 and 18, a first source/drain region (22 or 24) and a second source/drain region (24 or 22) separated by a channel region (no number) in a substrate, also as detailed above. The reference further

Art Unit: 2818

discloses that the asymmetrical low tunnel barrier intergate insulator has a number of small compositional ranges (“the dielectric film 18A is formed of a solid solution of two kinds of metal oxides, and the proportions of two metal oxides vary continuously from the bottom plane adjacent to the floating gate 16 to the top plane”, column 7, lines 1-8). However, the reference does not disclose a body region including the channel region and that the body region including the channel region is formed on the first source/drain region. In other words, the reference discloses a “planar” non volatile memory cell instead of a vertical non volatile memory cell as claimed.

Orlowski, in disclosing also a non volatile memory cell including a pair of source/drain regions, a channel region, a floating gate, and a control gate, teaches that vertical non volatile memory cell offers many advantages over a planar non volatile memory cell such as space saving, improved performance, reduced masking steps, and fully inverted or fully depleted channel regions (column 14, first paragraph). Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the reference’s non volatile memory cell such that it has a vertical configuration. One would have been motivated to make such a change because a vertical non volatile memory cell offers many advantages over a planar non volatile memory cell such as space saving, improved performance, reduced masking steps, and fully inverted or fully depleted channel regions, as taught by Orlowski.

Referring to **claim 11**, the ‘051 reference’s material (SrTiO_3 , column 7, lines 9-12) for the asymmetrical low tunnel barrier intergate insulator meets the limitation of the claimed Markush group of materials.

Referring to **claims 12-13**, the '051 reference discloses a non volatile memory cell substantially as claimed including the asymmetrical low tunnel barrier intergate insulator 18A including a number of small compositional ranges arranged in a "vary continuously" from the bottom surface to the top surface. The reference further teaches that the floating gate includes a polysilicon floating gate having a metal silicide formed thereon (column 3, lines 56-63) in contact with the asymmetrical low tunnel barrier intergate insulator, and that the control gate includes a metal control gate having a metal oxide layer formed thereon in contact with the asymmetrical low tunnel barrier intergate insulator.

Compared with the claims, the reference discloses a metal silicide instead of the claimed first metal layer for the floating gate, a metal oxide/metal instead of the claimed second metal/polysilicon for the control gate. However, the differences are deemed to be obvious to one of ordinary skill in the art at the time the invention was made ("the artisan") because at least one of the following two reasons: (1) the materials are known and available to the artisan; (2) both the present invention and the reference fails to show an advantage of one combination of materials to the other.

With respect to the limitation "wherein the metal layer includes a metal layer that has a different work function than the metal layer formed on the floating gate", the limitation appears to be inherent in the reference because: (1) the metal of the metal silicide (functionally equivalent to the claimed first metal) and the metal of the metal oxide (functionally equivalent to the claimed second metal) are different metals, resulting in different work functions; (2) the paragraph bridging columns 7 and 8, as noted above, expressly states that the barrier heights at the two surfaces of the asymmetrical low tunnel barrier intergate insulator, where the metal

Art Unit: 2818

silicide and the metal oxide are respectively in contact with, ought to be different, leading the artisan to conclude that the work function of the metal silicide (functionally equivalent to the claimed first metal) should be different from the work function of the metal oxide (functionally equivalent to the claimed second metal).

Referring to **claims 14 and 15**, the device of the '051 reference modified in view of Werkhoven and Orlowski thus comprises a vertical floating gate (such as 30, Orlowski's Fig. 1 or Fig. 10) along side a body region (22 or 58), and a vertical control gate (32) along side the vertical floating gate.

4. Claims 5 and 6 are rejected under 35 U.S.C. 103(a) as being unpatentable over Endo U.S. Patent 5,619,051 (the '051 reference) in view of Werkhoven et al. U.S. Patent Application Publication 20010041250 as applied to claim 1 above, and further in view of Eguchi et al. U.S. Patent 5,618,761 (cited in a previous office action).

The '051 reference in view of Werkhoven discloses a non volatile memory cell substantially as claimed and as detailed above including the graded asymmetrical low tunnel barrier intergate insulator 18A. The reference further discloses that the graded asymmetrical low tunnel barrier intergate insulator is formed of SrTiO_3 (column 7, lines 9-12), meeting the limitation of the claimed Markush group of materials of claim 6. The reference further discloses that the graded asymmetrical low tunnel barrier intergate insulator ought to have a high dielectric constant (the table in column 6, lines 35-45, and claim 1). However, the reference does not mention the limitation "Perovskite" for the graded asymmetrical low tunnel barrier intergate insulator.

Art Unit: 2818

Eguchi, in disclosing an insulator layer for a capacitor, mentions that a layer comprising Sr, Ti, and O having a perovskite crystal structure, which offers a high dielectric constant and excellent insulating properties (column 9, lines 37-45). Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the '051 reference's graded asymmetrical oxide tunnel barrier intergate insulator such that it is an asymmetrical Perovskite oxide tunnel barrier intergate insulator. One would have been motivated to make such a change because perovskite crystal structure offers a high dielectric constant and excellent insulating properties, which high dielectric constant property is desired by the '051 reference and which is taught by Eguchi.

5. **Claims 2, 20-22, and 85-86** are rejected under 35 U.S.C. 103(a) as being unpatentable over Endo U.S. Patent 5,619,051 (the '051 patent) in view of Werkhoven and further in view of Shinkawata et al. U.S. Patent Application Publication 20020008324 (cited in a previous office action).

The '051 reference in view of Werkhoven discloses a non volatile memory cell substantially as claimed and as detailed above for claims 1, 6, 10, and 18 including the graded asymmetrical low tunnel barrier intergate insulator 18A including a number of small compositional ranges arranged in a "vary continuously" from the bottom surface to the top surface, and wherein the number of small compositional ranges arranged in a "vary continuously" includes SrTiO_3 (column 7, lines 1-12). The materials for the second metal (in reference to claims 20 and 21) should also be known and available to the artisan as noted above.

However, instead of the claimed aluminum oxide (Al_2O_3), as noted, the reference discloses SrTiO_3 .

Shinkawata, in disclosing a gate insulating film 24 for semiconductor device, teaches that the two materials are equivalent (paragraph [0063]) (and they should be because otherwise the claimed device of claims 6, 11, 20-22, which contains both materials, would be inoperable).

Therefore, it would have been obvious to one of ordinary skill in the art the time the invention was made to form the '051 patent's asymmetrical low tunnel barrier intergate insulator such that it includes aluminum oxide (Al_2O_3) instead of SrTiO_3 . One would be motivated to do that as a choice of available and equivalent materials.

Allowable Subject Matter

6. **Claims 16-17, 19, and 87-95** are allowable over the prior art of record.

The following is an examiner's statement of reasons for the indication of allowable subject matter: The cited art, whether taken singularly or in combination, especially when all limitations are considered within the claimed specific combination, fails to teach or render obvious a non-volatile memory cell having all exclusive limitations as recited in claims 16 and 19, characterized in the limitations of claims 16 and 19 respectively.

Conclusion

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tu-Tu Ho whose telephone number is (571) 272-1778. The examiner can normally be reached on 7:30 am - 6:00 pm.

Art Unit: 2818

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, DAVID NELMS can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Tu-Tu Ho
March 21, 2006